I Claim:

1. An integrated, tunable capacitor, comprising:

a semiconductor body including a semiconductor region of a first conductivity type;

a first insulating region adjoining said semiconductor region of said first conductivity type;

a control electrode for applying a control voltage, said control electrode configured on said first insulating region;

a first region of a second conductivity type, said first region introduced into said semiconductor body, said first region adjoining said semiconductor region, said first region including a highly doped region of said second conductivity type, said highly doped region of said second conductivity type being highly doped with respect to said first region, said highly doped region of said second conductivity type for obtaining a tuning voltage; and

a well region of said second conductivity type, said well region configured in said first region of said second conductivity type, said well region configured below said highly doped region of said second conductivity type;

said highly doped region of said second conductivity type embodied as a terminal region.

2. The capacitor according to claim 1, further comprising:

a second region of said second conductivity type;

said second region of said second conductivity type configured symmetrically with respect to said first region;

said second region of said second conductivity type including a highly doped region for obtaining a control voltage;

said highly doped region of said second region being highly doped with respect to other regions of said second region;

said first region having a layer thickness; and

said second region of said second conductivity type having a layer thickness equal to said layer thickness of said first region.

3. The capacitor according to claim 1, further comprising:

a second insulating region introduced into said semiconductor body between said first region and portions of said

semiconductor region of said first conductivity type configured below said control electrode.

4. The capacitor according to claim 3, wherein:

said second insulating region has a layer thickness; and

said first region of said second conductivity type has a layer thickness that is greater than said layer thickness of said second insulating region.

5. The capacitor according to claim 1, further comprising:

a region for connecting to a reference-ground potential;

said region for connecting to the reference-ground potential being of said first conductivity type and being highly doped;

said region for connecting to the reference-ground potential introduced into said semiconductor body;

said region for connecting to the reference-ground potential adjoining said semiconductor region below said control electrode.

6. The capacitor according to claim 1, wherein:

said first region has a common interface with said first insulating region and said semiconductor region below said control electrode.

7. The capacitor according to claim 1, wherein:

said first region has a layer thickness that is greater than a maximum depth of a space charge zone that would be established by applying variable control voltage to another structure including:

a semiconductor body having a semiconductor region of said first conductivity type, a first insulating region adjoining said semiconductor region, and a control electrode configured on said first insulating region, said control electrode being supplied with the variable control voltage.

8. An integrated, tunable capacitor, comprising:

a semiconductor body including a semiconductor region of a first conductivity type;

a first insulating region adjoining said semiconductor region of said first conductivity type;

a control electrode for applying a control voltage, said control electrode configured on said first insulating region;

a first region of a second conductivity type, said first region introduced into said semiconductor body, said first region adjoining said semiconductor region, said first region including a highly doped region of said second conductivity type, said highly doped region of said second conductivity type being highly doped with respect to said first region, said highly doped region of said second conductivity type for obtaining a tuning voltage; and

a buried layer formed completely as a highly doped region;

said buried layer adjoining said first region of said second conductivity type.

9. The capacitor according to claim 8, wherein:

said first region is formed as a collector deep implantation region using bipolar fabrication technology.

10. The capacitor according to claim 8, further comprising:

a second region of said second conductivity type;

said second region of said second conductivity type configured symmetrically with respect to said first region;

said second region of said second conductivity type including a highly doped region for obtaining a control voltage;

said highly doped region of said second region being highly doped with respect to other regions of said second region;

said first region having a layer thickness; and

said second region of said second conductivity type having a layer thickness equal to said layer thickness of said first region.

11. The capacitor according to claim 8, further comprising:

a second insulating region introduced into said semiconductor body between said first region and portions of said semiconductor region of said first conductivity type configured below said control electrode.

12. The capacitor according to claim 11, wherein:

said second insulating region has a layer thickness; and

said first region of said second conductivity type has a layer thickness that is greater than said layer thickness of said second insulating region.

13. The capacitor according to claim 8, further comprising:

a region for connecting to a reference-ground potential;

said region for connecting to the reference-ground potential being of said first conductivity type and being highly doped;

said region for connecting to the reference-ground potential introduced into said semiconductor body;

said region for connecting to the reference-ground potential adjoining said semiconductor region below said control electrode.

14. The capacitor according to claim 8, wherein:

said first region has a common interface with said first insulating region and said semiconductor region below said control electrode.

15. The capacitor according to claim 8, wherein:

said first region has a layer thickness that is greater than a maximum depth of a space charge zone that would be established by applying variable control voltage to another structure including:

a semiconductor body having a semiconductor region of said first conductivity type, a first insulating region adjoining said semiconductor region, and a control electrode configured on said first insulating region, said control electrode being supplied with the variable control voltage.